ABSTRACT OF THE DISCLOSURE

A dual system includes a 0-subsystem and a 1-subsystem, each of which in turn includes a first bus, a second bus, a main memory having a memory section reading from and writing into which is performed over the first bus, a cache memory, a processor for outputting a first command for instruction to write back data of the cache memory into the main memory, a cache memory control section having a first reset terminal, through which an element thereof takes part in control of the first bus, for performing write back processing of data of the cache memory into the main memory based on the first command, and a system control section for controlling system changeover between an act system and a standby system over the system confounding line.